Paper No. 13

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte JON CHEEK, DERICK WRISTERS, and MARK I. GARDNER

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Appeal No. 2001-1419
Application No. 09/199,960

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ON BRIEF

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Before BARRETT, RUGGIERO, and BLANKENSHIP, Administrative Patent Judges.

RUGGIERO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal from the final rejection of claims 9-17. In the final rejection mailed May 24, 2000 (Paper No. 5), the Examiner indicated that claims 21-25 were allowed and that claims 18-20 contained allowable subject matter but were objected to as being dependent on a rejected claim. Claims 1-8 stand withdrawn from consideration as being drawn to a non-elected invention. An amendment filed July 25, 2000 after final rejection was approved for entry by the Examiner.

The disclosed invention relates to a process for manufacturing a semiconductor structure in which a polysilicon alignment structure is initially formed on a semiconductor substrate. Lightly doped drain regions are thereafter formed in the substrate structure and aligned with the alignment structure. After nitride spacers are formed on the sides of the alignment structure, source and drain regions are formed in the substrate and are aligned with the alignment structure. An epitaxial layer is grown on the substrate adjacent the spacers, and a trench is formed between the spacers by removing the polysilicon alignment structure. After a gate dielectric is formed in the trench and a silicide layer is formed on the epitaxial layer, a metal gate electrode is formed in the trench.

Claim 9 is illustrative of the invention and reads as follows:

> 9. A process for making a semiconductor structure with a silicon substrate, comprising:
>
> forming a polysilicon alignment structure on the substrate;
>
> implanting into the substrate at a first energy level a first concentration of a first dopant species, whereby lightly doped drain regions are formed in the substrate and aligned with the alignment structure;
>
> forming nitride spacers on sides of the alignment structure;

implanting into the substrate at a second energy level a second concentration of a second dopant species, whereby source and drain regions are formed in the substrate and aligned with the alignment structure;

growing an epitaxial layer on the substrate adjacent to the spacers;

removing the polysilicon alignment structure, thereby forming a trench between the spacers;

forming a gate dielectric in the trench;

forming a silicide layer on the epitaxial layer; and

forming a metal gate electrode in the trench, wherein the top of the gate electrode is disposed only over the lightly doped drain regions.

The Examiner relies on the following prior art:

Rodder et al. (Rodder) 5,198,378 Mar. 30, 1993

Stanley Wolf (Wolf), Silicon Processing for the VLSI Era, pp. 144-51, 157-58 (Lattice Press, Sunset Beach, CA 1990).

A. Chatterjee et al. (Chatterjee), "Sub-100 nm gate length metal gate NMOS transistors fabricated by a replacement gate process," International Electron Devices Meeting, 1997. Technical Digest., Int'l, pp. 33.1.1-33.1.4 (Dec. 1997).

Claims 9-17 stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Chatterjee in view of Rodder and Wolf.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the Briefs,[1] the final Office action, and the Answer for the respective details.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the Examiner, the arguments in support of the rejection, and the evidence of obviousness relied upon by the Examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, Appellants' arguments set forth in the Briefs along with the Examiner's rationale in support of the rejection and arguments in rebuttal set forth in the Examiner's Answer.

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would have suggested to one of ordinary skill in the art the obviousness of the invention as set forth in claims 9-17. Accordingly, we affirm.

We note that Appellants indicate at page 3 of the Brief that, for the purposes of this appeal, the appealed rejected

[1] The Appeal Brief was filed October 30, 2000 (Paper No. 9) in response to the final Office action mailed May 24, 2000 (Paper No. 5). In response to the Examiner's Answer mailed November 27, 2000 (Paper No. 10), a Reply Brief was filed January 31, 2001 (Paper No. 11), which was acknowledged and entered by the Examiner in the communication dated February 9, 2001 (Paper No. 12).

claims 9-17 form a single group. Consistent with this indication, Appellants have only argued limitations which are present in independent claim 9. For purposes of this appeal, we will consider claim 9 as representative of all of the claims on appeal, and the appealed claims 9-17 will all stand or fall together. Note In re King, 801 F.2d 1324, 1325, 231 USPQ 136, 137 (Fed. Cir. 1986); In re Sernaker, 702 F.2d 989, 991, 217 USPQ 1, 3 (Fed. Cir. 1983).

With respect to representative independent claim 9, the Examiner, as the basis for the obviousness rejection, proposes to modify the semiconductor structure fabrication process disclosure of Chatterjee. According to the Examiner, Chatterjee discloses the claimed invention except for " . . . the formation of elevated source/drain regions by growth of an epitaxial layer of silicon adjacent the spacers and forming a silicide on said epitaxial layers." (Answer, page 3, which makes reference to page 2 of the final Office action mailed May 24, 2000, Paper No. 5). To address this deficiency, the Examiner turns to Wolf and Rodder which disclose semiconductor structures having elevated source/drain regions with silicides formed thereon. In the Examiner's analysis, the skilled artisan would have been motivated and found it obvious to " . . . use the process as

disclosed by Chatterjee with the silicided, elevated source/drain regions taught by Rodder et al. and Wolf, because both Wolf and Rodder et al. teach the benefits of elevated source/drain regions." (Final Office action, page 2).

With respect to representative independent claim 9, after reviewing the Examiner's analysis, it is our view that such analysis points out the teachings of the Chatterjee, Rodder, and Wolf references, reasonably indicates the perceived differences between this prior art and the claimed invention, and provides reasons as to how and why the prior art teachings would have been modified and/or combined to arrive at the claimed invention. In our opinion, the Examiner's analysis is sufficiently reasonable that we find that the Examiner has at least satisfied the burden of presenting a prima facie case of obviousness. The burden is, therefore, upon Appellants to come forward with evidence and/or arguments which persuasively rebut the Examiner's prima facie case of obviousness. Only those arguments actually made by Appellants have been considered in this decision. Arguments which Appellants could have made but chose not to make in the Brief have not been considered (see 37 CFR § 1.192(a)).

In response, Appellants offer several arguments in support of their contention that the Examiner has failed to establish a

prima facie case of obviousness. Initially, Appellants contend (Brief, page 4; Reply Brief, pages 2 and 3) that the Examiner has misinterpreted the Chatterjee reference as disclosing a gate electrode that does not extend past the LDD (lightly doped drain) regions or, in the words of claim 9, " . . . wherein the top of the gate electrode is disposed only over the lightly doped drain regions."

After careful review of the applied prior art references in light of the arguments of record, we are in general agreement with the Examiner's analysis and position as stated in the final Office action and the Answer. As asserted by the Examiner, the pictures of an actual semiconductor device which make up Figure 2 of Chatterjee show at least the right side of the gate electrode extending not quite as far as the edge of the spacer. Further, although Chatterjee is silent about the fabrication processing for forming the LDD regions, it is apparent to us from the evidence of record, including Appellants' own arguments (Brief, page 4), that the conventional manner of forming semiconductor gate and source/drain regions is to initially form LDD regions, aligned with an alignment structure, in a substrate. Sidewall spacers aligned with the alignment structure are then formed over the LDD regions which act as a mask for the

subsequent formation of more heavily doped source/drain regions. We conclude therefore that at least the right side of the top of the pictured gate electrode in Chatterjee's Figure 2 extends only over the LDD region.

It is further our view that, although the Figure 2 picture of the top left side of the gate electrode in Chatterjee arguably overlaps the spacer edge, the only reasonable conclusion from the entirety of the disclosure of Chatterjee, whose textual description is silent about the extent of the top of the gate electrode, is that the skilled artisan would recognize and appreciate the obviousness of extending the gate electrode to any distance over the source/drain regions. In other words, the gate electrode could obviously overlap the spacer on one side and not the other or not overlap at all, i.e., so that it extends only over the LDD regions as in Appellants' claims. Appellants have presented no evidence to rebut the presumption of obviousness of this feature and, as asserted by the Examiner, Appellants' own specification has no written disclosure to support the criticality of the gate electrode extent feature. In fact, since Appellants' written disclosure has no description at all of such gate electrode coverage feature, we can only conclude that Appellants' only rationale for limiting the extent of the top of

the gate electrode is as a result of an incidental illustration in Figure 4 in Appellants' drawings. Given this lack of evidentiary support by Appellants, we find that Appellants' arguments are not sufficient to overcome the presumption of obviousness to the skilled artisan of placing the top of the electrode gate so that it is disposed only over the LDD regions as claimed.

We also find to be unpersuasive Appellants' contention (Brief, pages 4 and 5) that the Examiner's proposed modification of Chatterjee, in which the source/drain regions are silicided as taught by Rodder and Wolf, would electrically short out the gate electrode and thereby render Chatterjee unsatisfactory for its intended purpose. It is apparent to us from reviewing the Examiner's analysis that the Examiner is not suggesting the bodily incorporation of the silicided structures of Rodder and Wolf into the device of Chatterjee. Rather, it is the disclosed advantages of utilizing an elevated silicided source/drain structure that is being relied upon as a suggestion for the proposed combination. "The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference . . . . Rather, the test is what the combined teachings of those references would

have suggested to those of ordinary skill in the art." In re Keller, 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981). See also In re Sneed, 710 F.2d 1544, 1550, 218 USPQ 385, 389 (Fed. Cir. 1983) and In re Nievelt, 482 F.2d 965, 968, 179 USPQ 224, 226 (CCPA 1973).

Further, it is a basic tenet of patent law that skill of an artisan working in a particular field of endeavor is to be presumed. In re Sovish, 769 F.2d 738, 743, 226 USPQ 771, 774 (Fed. Cir. 1985). The factual situation presented to us here leads us to the finding that the artisan working in the field of semiconductor fabrication, given the clear motivation provided by Rodder and Wolf to implement silicided elevated source/drain technology in the device of Chatterjee, would know how to construct a device structure so that electrical shorts do not occur. It is further our view that, in contrast to Appellants' contention, the TiN layer in Chatterjee would serve as a protection against any contact with the gate that might cause an electrical short. We would also point out that Rodder, as illustrated in Figure 8, had no difficulty in constructing a gate structure in which a metal contact 36 is incorporated into a device with a silicided region 34.

For the above reasons, since it is our opinion that the Examiner's prima facie case of obviousness has not been overcome by any convincing arguments from Appellants, the Examiner's 35 U.S.C. § 103(a) rejection of representative independent claim 9, as well as dependent claims 10-17 which fall with claim 9, is sustained.

In summary, we have sustained the Examiner's 35 U.S.C. § 103(a) rejection of all of the claims on appeal. Therefore, the decision of the Examiner rejecting claims 9-17 is affirmed.[2]

[2] At page 10 of the Answer, the Examiner asserts a possible enablement problem with claims 18-20 which presently stand objected to and which Appellants have amended to place in independent form. As there is no 35 U.S.C. § 112, first paragraph, rejection of these claims before us, we decline to rule on the merits of such assertion.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

LEE E. BARRETT Administrative Patent Judge	)	
JOSEPH F. RUGGIERO Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
HOWARD B. BLANKENSHIP Administrative Patent Judge	)	

JFR:hh

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